What is claimed is:

1. A flat panel display device comprising:

a first substrate including a plurality of scanning lines, and a plurality of signal lines intersecting the scanning lines, a switching element arranged on an intersection point of each of the scanning lines and the signal lines, a pixel electrode connected to said switching element;

a second substrate including an opposite electrode opposite to said pixel electrode;

a display layer held between said first and second substrates;

a data driver which supplies a data signal to each of said signal lines; and

a scan driver which supplies a scanning signal to each of said scanning lines,

wherein a control signal and a power source voltage are supplied from an external control circuit to said data driver and said scan driver, and

wherein at least one pumping circuit included in said external control circuit is arranged on said first substrate, and a first capacitor connected to a clock input portion of said pumping circuit and a second capacitor connected between an output portion and the ground are arranged outside said first substrate.

2. The flat panel display device according to claim 1, wherein at least one of said first and second capacitors is arranged inside said external control circuit.

3. The flat panel display device according to claim 1, wherein a capacitance component of an auxiliary capacitor connected in parallel to said pixel electrode is included in said second capacitor.

4. A pumping circuit, comprising:

a first transistor having a first electrode region and a third electrode region, which are supplied with a power source voltage, and a second electrode region connected to a potential of a first intermediate node;

a second transistor having a first electrode region supplied with a power source voltage, a second electrode region connected to a potential of a second intermediate node and a third electrode region connected to the potential of said first intermediate node; and

a third transistor having a first electrode region connected to the potential of said second intermediate node, a second electrode region connected

to an output portion together with a third capacitor, and a third electrode region connected to the potential of said first intermediate node,

wherein a first clock input portion for receiving a first clock signal through a first capacitor is connected to said first intermediate node, and a second clock input portion for receiving a second clock signal through a second capacitor is connected to said second intermediate node.

5. The pumping circuit according to claim 4, wherein said first transistor and said second transistor are the ones of the same polarity, and said third transistor is the one of an opposite polarity to that of said first and second transistors.

6. The pumping circuit according to claim 4, wherein said second clock signal is an inverted clock signal obtained from said first clock signal.

7. A pumping circuit, wherein first and second transistors having opposite polarities are connected in series and two transistor pairs composed of the first and second transistors are connected in series.

8. A pumping circuit, wherein first and second transistors having opposite polarities are connected in parallel and two transistor pairs composed of the first and second transistors are connected in series.

9. A pumping circuit, comprising:

a first pumping circuit in which a first transistor of a first conductivity type and a second transistor of a second conductivity type are connected in series, and two transistor pairs composed of the first and second transistors are in series connected;

a second pumping circuit in which a first transistor of the second conductivity type and a second transistor of the first conductivity type are connected in series, and transistor pairs composed of the first and second transistors are in series connected; and

an operational amplifier which receives an output from said first pumping circuit as a positive polarity power source and an output from said second pumping circuit as a negative polarity power source.

10. The flat panel display device according to claim 1, wherein a control signal supplied from said external control circuit to said data driver and said scan driver is supplied also to said pumping circuit.

11. The flat panel display device according to claim 10,

said device further comprising:

a level shift circuit for changing a voltage level of the control signal

supplied to said pumping circuit to a predetermined voltage level.

12. The flat panel display device according to claim 10,

said device further comprising:

a frequency dividing circuit for changing a frequency of the control signal supplied to said pumping circuit to a predetermined frequency.

13. The flat panel display device according to claim 10, wherein said control signal is one of a horizontal clock signal supplied to said data driver and a horizontal start signal supplied thereto.

14. The flat panel display device according to claim 10, wherein said control signal is one of a vertical clock signal supplied to said scan driver and a vertical start signal supplied thereto.

15. The flat panel display device according to claim 10, wherein one of the control signal supplied to said data driver and the control signal supplied to said scan driver is selectively supplied to said pumping circuit in accordance with an operation state of said pumping circuit.

16. The flat panel display device according to claim 15, wherein when said pumping circuit is in a standby state in which said pumping circuit is not performing a boosting operation, the control signal supplied to said scan driver is selected, and when said pumping circuit is an active state in which said pumping circuit is performing the boosting operation, the control signal supplied to said data driver is selected.

17. The flat panel display device according to claim 1, wherein the power source voltage supplied from said external control circuit to said data driver and said scan driver is supplied also to said pumping circuit.

18. A flat panel display device comprising:

a first substrate including a plurality of scanning lines, and a plurality of signal lines intersecting the scanning lines, a switching element arranged on an intersection point of each of the scanning lines and the signal lines, a pixel electrode connected to said switching element;

a second substrate including an opposite electrode opposite to said pixel electrode;

a display layer held between said first and second substrates;

a data driver which supplies a data signal to each of said signal lines; and

a scan driver which supplies a scanning signal to each of said scanning

lines,

wherein a control signal and a power source voltage are supplied from an external control circuit to said data driver and said scan driver, and

wherein at least one pumping circuit included in said external control circuit is arranged in a region opposite to a region in which said scan driver on said first substrate is arranged.

19. The flat panel display device according to claim 18, wherein a bypass capacitor is arranged instead of said pumping circuit.